

### **high speed cmos design pdf**

Design of a high-speed CMOS comparator. Author(s) Ahmad Shar . vii ABSTRACT This master thesis describes the design of high-speed latched comparator with 6-bit resolution, full scale voltage of 1.6 V and the sampling frequency of 250 MHz. The comparator is designed in a 0.35 9m CMOS process with a

### **DESIGN OF A HIGH-SPEED CMOS COMPARATOR**

Proposed design exhibits reduced delay and high speed with a 1.0 V supply. This design can be used where high speed and low propagation delay are the main parameters. Simulation The design is simulated in the design is simulated in 0.25 $\mu$ m CMOS Technology using Tanner EDA Tools. Comparator design shows reduced delay and high speed with a 1.0 V supply.

### **Design and Simulation of a High Speed CMOS Comparator**

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94 Design of Low Power and High Speed CMOS Comparator for A/D Converter Application . Figure 6. Result for power dissipation. Table 1. Comparison of present results with earlier reported work.

### **Design of Low Power and High Speed CMOS Comparator for A/D**

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DESIGN OF HIGH-SPEED SERIAL LINKS IN CMOS Chih-Kong Ken Yang Technical Report No. CSL-TR-98-775 December 1998 Sponsored by Center for Integrated Systems, Sun Microsystems, and LSI Logic Inc.

### **DESIGN OF HIGH-SPEED SERIAL LINKS IN CMOS**

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